

TITLE 1.6T OSFP Active Electrical Cable - PAM4	DOC No. RFD-20260115001-002	
	REVISION : 01	AUTHORIZED BY : Hawk Rong
	DATE : 2026.01.15	CLASSIFICATION : Active Electrical Cable

1. Product Features

- Compliant with IEEE 802.3dj
- Compliant to OSFP MSA Rev 2.0
- Compliant with CMIS 5.0
- Transmission data rate up to PAM4 212.5Gbps per channel
- Single +3.3V power supply
- BER (Pre-FEC) <1E-8
- BER (Post-FEC) <1E-15
- Copper link up to max length 4.5m
- Support Integrated Heat Sink and Removable Heat Sink
- Supports device programming by MCU with I2C

2. Product Applications

- Switches, servers and routers
- Data Center networks
- Storage area networks
- High performance computing
- Telecommunication and wireless infrastructure
- Medical diagnostics and networking
- Test and measurement equipment
- Infiniband Interconnect

3. Industry Standards

- 1600G Ethernet(IEEE 802.3dj)
- InfiniBand XDR
- Compliant with CMIs 5.0

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4. Product Description

OSFP active electrical cable assembly feature sixteen differential copper pairs, providing eight data transmission channels at speeds up to 200Gbps(PAM4) per channel, and meets 1600G Ethernet and InfiniBand XDR requirements. Available in 25AWG to 30AWG wire gauges, this 1600G copper cable assembly features low insertion loss and low crosstalk.

4.1 Product Name And Series Number(s)

1.6T OSFP Active Electrical Cable - PAM4

JPC P/N	Length(m)	Cable AWG	Description
PAT**7W0a**M-1	1.0m – 2.0m	30 AWG	1600G (1.6T) OSFP AEC PAM4 30AWG **m
PAT**7X0a**M-1	1.0m – 3.0m	28 AWG	1600G (1.6T) OSFP AEC PAM4 28AWG **m
PAT**7Z0a**M-1	4.0m – 4.5m	25 AWG	1600G (1.6T) OSFP AEC PAM4 25AWG **m

Note-1 : ** Indicates the customer code.

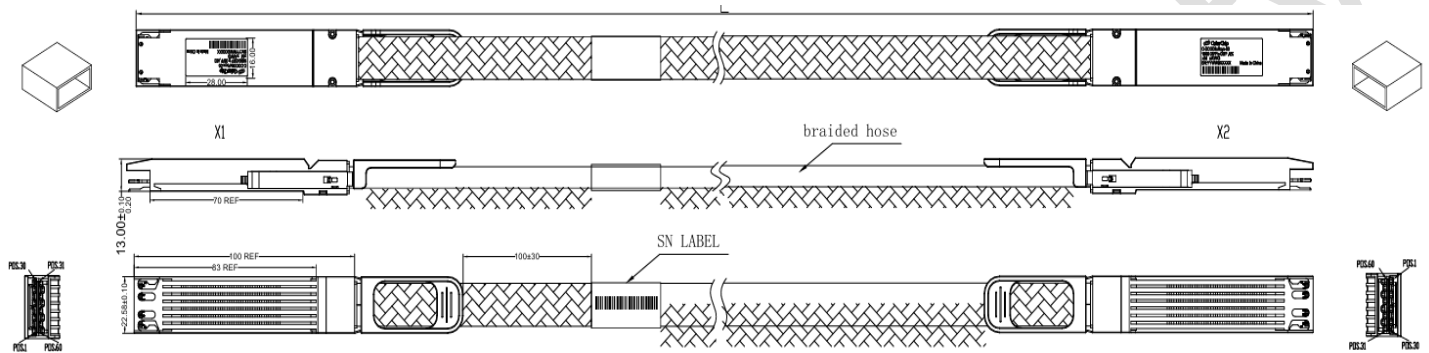
Note-2 : a Indicates the Housing Heat Sink

e.g. A means IHS-IHS, C means IHS-RHS

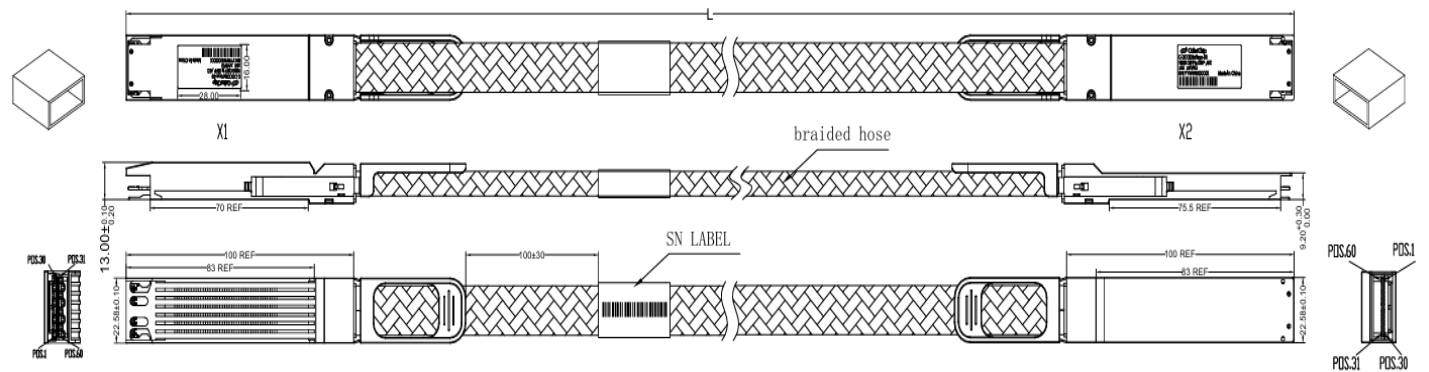
Note-3 : ** Indicates the length.

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4.2 DIMENSIONS, MATERIALS, PLATINGS AND MARKING



IHS to IHS Mechanical Dimensions



IHS to RHS Mechanical Dimensions

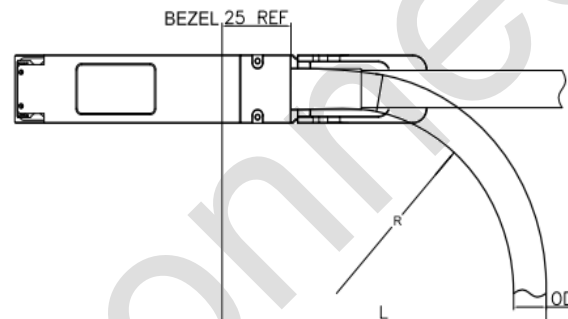
Length (m)	Cable AWG
0.5m – 2.0m	30/28
2.0m – 3.0m	28
4.0m - 4.5m	25

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Unit is millimeter. All dimensions are $\pm 0.1\text{mm}$ unless otherwise specified

Bending Radius Specifications

Wire gauge	OD(Ref)	Min. bend radius	Bend space
30AWG	9.5mm	19mm	64mm
28AWG	10.2mm	20.4mm	65mm
25AWG	11.4mm	28.5mm	73mm



5. General Product Characteristics

1600G OSFP AEC Specifications	
Number of Lanes	Tx8 & Rx8
Channel Data Rate	212.5Gbps
Operating Temperature	0 to + 70°C
Humidity	5 to 95%
Storage Temperature	-40 to + 85°C
Supply Voltage	3.3 V nominal
Electrical Interface	60pins edge connector

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Management Interface	Serial, I ² C
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6. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Case Temperature- Operating	T _{CASE}	0		70	°C
Supply Voltage	V _{CC}	3.135	3.3	3.465	V
Power Consumption	P _{DISS}			19	W
Pre-FEC Bit Error Ration				1x10 ⁻⁸	
Pre-FEC Bit Error Ration				1x10 ⁻¹⁵	
Date Rate			1600		Gbps

7. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical	MIL-STD-883C Method 3015.7	Class 1(>2000 Volts)
Electromagnetic Interference(EMI)	FCC Class B	Compliant with Standards
	CENELEC EN55022 Class B	
	CISPR22 ITE Class B	
RF Immunity(RFI)	IEC61000-4-3	Typically Show no Measurable Effect from a 10V/m Field Swept from

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RoHS Compliance	RoHS Directive 2011/65/EU and it's Amendment Directives (EU) 2015/863	RoHS (EU) 2015/863 compliant
REACH Compliance	REACH Regulation (EC) No 1907/2006	REACH (EC) No 1907/2006 compliant

8. Applications Note:

Pin Definitions

Top Side (viewed from top)

60	GND	
59	TX1p	
58	TX1n	
57	GND	
56	TX3p	
55	TX3n	
54	GND	
53	TX5p	
52	TX5n	
51	GND	
50	TX7p	
49	TX7n	
48	GND	
47	SDA	
46	VCC	
45	VCC	
44	INT/RSTn	
43	GND	
42	RX8n	
41	RX8p	
40	GND	
39	RX6n	
38	RX6p	
37	GND	
36	RX4n	
35	RX4p	
34	GND	
33	RX2n	
32	RX2p	
31	GND	

Module Card Edge

Bottom Side (viewed from bottom)

	GND	1
	TX2p	2
	TX2n	3
	GND	4
	TX4p	5
	TX4n	6
	GND	7
	TX6p	8
	TX6n	9
	GND	10
	TX8p	11
	TX8n	12
	GND	13
	SCL	14
	VCC	15
	VCC	16
	LPWn/PRSn	17
	GND	18
	RX7n	19
	RX7p	20
	GND	21
	RX5n	22
	RX5p	23
	GND	24
	RX3n	25
	RX3p	26
	GND	27
	RX1n	28
	RX1p	29
	GND	30

Pin Function Definitions

Pin	Logic	Symbol	Description
1		GND	Ground

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2	CML-I	Tx2p	Transmitter Non-Inverted Data Input
3	CML-I	Tx2n	Transmitter Inverted Data Input
4		GND	Ground
5	CML-I	Tx4p	Transmitter Non-Inverted Data Input
6	CML-I	Tx4n	Transmitter Inverted Data Input
7		GND	Ground
8	CML-I	Tx6p	Transmitter Non-Inverted Data Input
9	CML-I	Tx6n	Transmitter Inverted Data Input
10		GND	Ground
11	CML-I	Tx6p	Transmitter Non-Inverted Data Input
12	CML-I	Tx6n	Transmitter Inverted Data Input
13		GND	Ground
14	LVC MOS-I/O	SCL	2-wire serial interface clock
15		VCC	+3.3V Power supply
16		VCC	+3.3V Power supply
17		LPWn/PRSn	Low-Power Mode / Module Present
18		GND	Ground
19	CML-O	Rx7n	Receiver Inverted Data Output
20	CML-O	Rx7p	Receiver Non-Inverted Data Output
21		GND	Ground
22	CML-O	Rx5n	Receiver Inverted Data Output
23	CML-O	Rx5p	Receiver Non-Inverted Data Output
24		GND	Ground
25	CML-O	Rx3n	Receiver Inverted Data Output
26	CML-O	Rx3p	Receiver Non-Inverted Data Output
27		GND	Ground
28	CML-O	Rx1n	Receiver Inverted Data Output
29	CML-O	Rx1p	Receiver Non-Inverted Data Output
30		GND	Ground
31		GND	Ground
32	CML-O	Rx2p	Receiver Non-Inverted Data Output
33	CML-O	Rx2n	Receiver Inverted Data Output
34		GND	Ground
35	CML-O	Rx4p	Receiver Non-Inverted Data Output
36	CML-O	Rx4n	Receiver Inverted Data Output

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37		GND	Ground
38	CML-O	Rx6p	Receiver Non-Inverted Data Output
39	CML-O	Rx6n	Receiver Inverted Data Output
40		GND	Ground
41	CML-O	Rx8p	Receiver Non-Inverted Data Output
42	CML-O	Rx8n	Receiver Inverted Data Output
43		GND	Ground
44		INT/RSTn	Module Interrupt / Module Reset
45		VCC	+3.3V Power supply
46		VCC	+3.3V Power supply
47	LVCMOS-I/O	SDA	2-wire serial interface data
48		GND	Ground
49	CML-I	Tx7n	Transmitter Inverted Data
50	CML-I	Tx7p	Input Transmitter Non-Inverted Data Input
51		GND	Ground
52	CML-I	Tx5n	Transmitter Inverted Data
53	CML-I	Tx5p	Input Transmitter Non-Inverted Data Input
54		GND	Ground
55	CML-I	Tx3n	Transmitter Inverted Data
56	CML-I	Tx3p	Input Transmitter Non-Inverted Data Input
57		GND	Ground
58	CML-I	Tx1n	Transmitter Inverted Data
59	CML-I	Tx1p	Input Transmitter Non-Inverted Data Input
60		GND	Ground

9. Modification History

Rev.	Comments	Date	Originator	Approval
01	Initial	2026.01.15	Hawk Rong	Mike Sun